IN THE CLAIMS

Please cancel claims 1-20 and add the attached new claims 21-40.

REMARKS

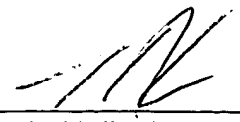
Prior to a formal examination of the above-identified application, acceptance of the new claims and the enclosed substitute specification (under 37 CFR 1.125) is respectfully requested. It is believed that the substitute specification and the new claims will facilitate processing of the application in accordance with M.P.E.P. 608.01(q). The substitute specification and the new claims are in compliance with 37 CFR 1.52 (a and b) and, while making no substantive changes, are submitted to conform this case to the formal requirements and long-established formal standards of U.S. Patent Office practice, and to provide improved idiom and better grammatical form.

The enclosed substitute specification is presented herein in both marked-up and clean versions.

STATEMENT

The undersigned, an agent registered to practice before the Office, hereby states that the enclosed substitute specification includes the same changes as are indicated in the marked-up copy of the original specification. It does not contain new subject matter.

Respectfully submitted,



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SUBSTITUTE SPECIFICATION: MARKED COPY

Device and Method for Analyzing Embedded Systems

BACKGROUND OF THE INVENTION

[0001] The present invention relates to an analysis device for ~~according to the preamble of claim 1~~, an embedded system ~~according to the preamble of claim 12~~, and a method for the analysis of an embedded system with an analysis device.

[0002] To successfully develop software for embedded systems, it is a general practice to provide devices enabling error detection during the operation time (debugging). In the known concept of debugging embedded systems by way of a so-called JTAG interface (Joint Test Action Group, IEEE Standard 1149.1-1990, 'IEEE Standard Test Access Port and Boundary Scan Architecture', Institute of Electrical and Electronics Engineers Inc., New York, USA, 1990) it is possible to perform testing operations by means of a 'Boundary-Scan' testing method. This method allows single-step processing of the processor (single stepping), the setting of break points (break points) and the setting of so-called watch points. Although these per se known auxiliary means for error detection permit monitoring the principal program execution and the condition of values of single variables, generally the running system must be stopped to this end. It is disadvantageous, however, that the output of the microcomputer can no longer be in real time.

[0003] The problem encountered is that embedded systems frequently are real time systems and, due to their typical range of application in real-time controls, do not allow being stopped for debugging purposes, not at least for checking the data changed in connection with the real time processing.

[0004] The so-called trace-interface is further known in the art, where the conduction of all relevant CPU bus signals (address signals, data signals and control signals) by way of housing pins e.g. to an external logic analysis device is enabled by using a 'bond-out' chip for the real time analysis. The bond-out chip is a microcontroller (MCU) in another casing, where the processor bus (data, address and control signals) is bonded towards the outside.

[0005] With the high system frequencies of several hundred megahertz being conventional nowadays for embedded systems and the modern memory architectures with caches, this method for the error analysis can no longer be used due to the high speed requirements. A real time output of relatively comprehensive data memories (for example, of a size of more than 100 kilobyte) is generally impossible due to the system frequencies predetermined on account of the technology employed and the resulting band width. One given possibility of creating the band width necessary for the real time data transfer would be a parallel output of the data to be transferred. However, the number of pins available for this purpose is normally limited, not least for cost reasons.

[0006] In view of the above, an object of the invention is to provide an analysis device for embedded systems, which can be employed also in the up-to-date quick embedded systems.

SUMMARY OF THE INVENTION

[0007] This object is achieved by ~~the~~ an analysis device ~~according to claim 1~~ having a CPU, a CPU bas, a memory and a communication module.

[0008] The invention is based on the following reflections: On the one hand, the internal system condition of an embedded system can be described or analyzed, respectively, by way of its present data memory contents (RAM). From this follows that in case this memory content can be copied in real time into an external data memory, there is a possibility of further processing and evaluating the system condition from this point by means of a subsequent evaluation unit.

[0009] In the analysis device a copy of the internal system condition is preferably written in real time into an external memory.

[0010] The analysis device is preferably part of an embedded system, which is employed in particular in electronic control devices for motor vehicle brake systems. In the embedded system according to the invention, preferably basic components of the system such as one or more CPUs and memories are designed partly or fully redundantly. The safety of operation of the embedded system is hereby enhanced.

[0011] Preferably, the logging of data does not take place in such a fashion that the entire memory content or the content of a whole memory range is transmitted. Rather, only the changes in the memory, especially all write access operations of the CPU and/or the periphery are transmitted. A reduction of the necessary band width for the data output can take place this way.

[0012] Further, the system preferably comprises a means for the direct data output by the CPU. Apart from this means for the direct data output, especially a means for an automatic replication of the data in the background by way of the analysis

module is provided. The result is the advantage of an increased flexibility in the data output.

[0013] Especially for these cases of application, the invention discloses a universal data input and output module configured in such a manner that in real time a data exchange can be carried out by means of an embedded system without having to stop (not even temporarily) this system (non-intrusive).

[0014] Compared to the software debugging devices known from the state of the art, the analysis device of the invention is advantageous in that in the development of control algorithms, e.g. for motor vehicle brake systems, the dynamic system behavior, especially the control variables, can be monitored during the debugging operation. It is furthermore favorable that a data input into the embedded system can be carried out for the employment of an embedded system in a hardware-in-the-loop simulator or in a rapid-prototyping system.

[0015] Another objective of the invention is a method for the analysis of an embedded system as described hereinabove with an analysis device ~~according to claim 12~~ having a CPU, a CPU bus, a memory and a communication module.

[0016] The method is advantageous in that the processing speed of the embedded system is not reduced on account of the debugging processes running in the background. This condition renders possible a real time processing of the data even during the debugging operation.

[0017] Preferably, the method of the invention also comprises steps for the output of the complete data memory contents in real time.

~~[0018] Further preferred embodiments can be seen in the sub claims.~~

BRIEF DESCRIPTION OF THE DRAWING

[0019] Figure 1 illustrates an analysis device.

DETAILED DESCRIPTION OF THE DRAWING

[0020] The analysis device of the invention and the method of the invention will be described in the following by way of embodiments while making reference to Figure 1.

[0021] Figure 1 shows an embedded system 9 with an analysis device 4 according to the invention.

[0022] The embedded system 9 comprises one or more CPUs 1, one RAM 3, an analysis device 4 and a debugging interface 5. To simplify the wiring diagram, further conventional functional elements of the embedded system such as ROM, clock generation, IO, etc., are not illustrated.

[0023] The analysis device includes three function modes that will be described hereinbelow. In function mode 1 the analysis device reads for control all write access operations of the CPU 1 to the data memory 3. This means all write access operations of the CPU 1 to the data memory 3 are written automatically by way of CPU bus 2 by the suggested extended data output/input unit 4 (EDP, Enhanced Data Port) by means of a controller contained therein by way of a parallel interface 5 to the external data

memory 6. To this end, the controller must have at least the same band width as the memory 3 used. Beside a connection to the data bus, the controller has in particular a connection to the control bus and to the address but in order that, according to a preferred embodiment of the method, only especially selected address ranges and/or especially selected data types can be monitored for the analysis. Accordingly, CPU 1 does not have to execute additional commands for tapping the data and for the data transfer.

[0024] The external data memory 6 is preferably designed as a dual-port memory and usually contains an exact reproduction of the memory ranges monitored in RAM 3 or the entire memory content of RAM 3, respectively. Memory 6 can also be a magnetic core memory storing the arriving data flow for a later (offline) analysis.

[0025] External interface 5 preferably has a band width that is smaller than the band width of the CPU bus. FIFO memory 8, which is arranged within the data output unit 4, ensures a time buffer of the tapped data. It is this way possible to output also accesses to interface 5 where a cache line or a CPU register dump is re-written upon entry into the function.

[0026] In the function mode 2 the analysis device 4 reads for control all reading access operations of CPU 1 to the data memory. This mode largely corresponds to function mode 1, however, there are the following differences: all reading access operations are automatically output by way of interface 5. Analysis unit 4 then registers all operations such as read cycles, write cycles, etc., which are visible on the CPU bus (read for control). In function mode 2 CPU 1 actively performs a

memory dump entailing, however, an insignificant tolerable loss in running time. Due to the analysis unit 4 reading for control, the number of clock cycles necessary for the output of data words for the analysis are reduced or even avoided, respectively.

[0027] CPU 1 reads the data memory content into the registers (not shown) of the CPU. The data available in the registers can then be written in analysis unit 4. The mode of function described herein basically corresponds to the function mode 3 that will be described hereinbelow.
In the analysis device suggested in the present example (function mode 2), CPU 1 reads the data memory content into the CPU registers. In parallel to this, the data output unit 4, which overhears the data bus, automatically outputs the corresponding data, i.e., there is no need for an explicit write cycle for the data output for the analysis.

[0028] In function mode 3 there is direct writing on the data output unit or direct reading from the data output unit. Thus, function mode 3 corresponds to function mode 1, apart from the fact that data is actively output by the CPU 1 externally to the analysis unit 4, or is read in actively from there, respectively, with the result, however, that additional clock cycles are necessary.

[0029] By way of module 7, the analysis unit can transfer data from the external memory 6 to typical debugging applications such as real-time monitoring of the system condition 10, offline analysis for creating a complete data memory reproduction by way of module 11, flash download by way of communication channel 12 (programming of the program memory), parameter variation during

the operation of the embedded system, transfer of system stimuli, rapid prototyping and hardware-in-the-loop simulation.

Patent Claims:

1. An analysis device for an embedded system (9) comprising a CPU (1), a CPU bus (2), and a memory (3), and including at least one communication module (4) for the input or output of analysis data by way of a test interface (5), c h a r a c t e r I z e d in that the communication module permits the internal memory and input and output access operations of the embedded system to be monitored and/or logged without using the clock cycles of the CPU (1).

2. The analysis device as claimed in claim 1, c h a r a c t e r i z e d by two, in particular at least three freely selectable analysis modes, with the analysis modes, in the way and extent of participation of the CPU 1, differing from each other in the read and/or write operations of data for analyzing purposes.

3. The analysis device as claimed in claim 2, c h a r a c t e r i z e d in that depending on the selected analysis mode, either
   - all write access operations of the CPU are logged to especially definable address ranges without using clock cycles, or
   - all read access operations of the CPU are logged, or
   - direct reading and writing of the CPU out of/into an external memory (6) is executed by using clock cycles.

4. The analysis device as claimed in at least one of claims 1 to 3,

c h a r a c t e r i z e d in that the communication module comprises a controller which, by way of a connection to the data bus and/or the control bus and/or the address bus, can independently make access to this bus/these buses of the embedded system in order to monitor write and/or read access operations in real time, that means without influencing of the CPU.

5. The analysis device as claimed in at least one of claims 1 to 4,
c h a r a c t e r i z e d in that the communication module is connected to a buffer store (8) or in particular comprises said, and the data transferred in write and/or read access operations can be stored in the buffer store.

6. The analysis device as claimed in at least one of claims 1 to 5,
c h a r a c t e r i z e d in that data can be output from the buffer store in a buffered fashion by way of test interface (5) or data can be read into the buffer store by way of this interface.

7. The analysis device as claimed in at least one of claims 1 to 6,
c h a r a c t e r i z e d in that the external test code memory (6) is a magnetic core memory or a dual-port memory.

8. The analysis device as claimed in at least one of claims 1 to 7,

c h a r a c t e r i z e d in that the communication module (4) is integrated into the embedded system.

9. The analysis device as claimed in at least one of claims 1 to 8,
c h a r a c t e r i z e d in that the test interface (5) is connected to a test code memory (6) arranged outside the embedded system.

10. The analysis device as claimed in at least one of claims 1 to 9,
c h a r a c t e r i z e d in that the data transfer from the communication module to the external memory takes place by way of a parallel interface.

11. The analysis device as claimed in at least one of claims 1 to 10,
c h a r a c t e r i z e d in that the external memory (6) is connected to a data conditioning device (7) providing an interface connection (14) to external debugging applications.

12. An embedded system comprising a central processor unit (1), a CPU bus (2) and a memory (3),
c h a r a c t e r i z e d in that the system comprises an analysis device as claimed in at least one of claims 1 to 11.

13. A method for the analysis of an embedded system with an analysis device as claimed in at least one of claims 1 to 11,
c h a r a c t e r i z e d in that at least one mode is provided in which the analysis data in real time can be read out of the system that comprises at least CPU, data memory,

program memory and input/output element(s), and/or can be written in the system so that the system need not be stopped or interrupted, respectively, for the analysis.

14. The method as claimed in claim 13,
c h a r a c t e r i z e d in that
- the memory content or a correspondingly assessable information of the embedded system, in whole or in part, is copied in real time into an external memory, with the data being buffered in particular before this operation, and/or
- the data content of an external memory (6) or a correspondingly assessable information about the memory content of the memory (6), in whole or in part, is copied in real time into a memory of the embedded system, with the data being buffered in particular before this operation.

15. The method as claimed in claim 13 or 14,
c h a r a c t e r i z e d in that the external memory is used to transmit data for typical debugging applications.

16. The method as claimed in at least any one of claims 13 to 15,
c h a r a c t e r i z e d in that only the data needed for debugging is transferred to the external memory (6) in the event of access operations of the CPU to RAM 3.

17. The method as claimed in at least any one of claims 13 to 16,

c h a r a c t e r i z e d in that write access operations and/or read access operations of the CPU are logged by means of a buffer store.

18. The method as claimed in claims 13 to 17, c h a r a c t e r i z e d in that information about the write access operations is written without additional CPU commands into the buffer store (8) or directly into the communication module (4), and the information about the read access operations is written into the buffer store with active assistance of the CPU.

19. The method as claimed in at least any one of claims 13 to 18, c h a r a c t e r i z e d in that a mode of the embedded system is provided in which all write and/or read access operations of the CPU are rerouted to the communication module.

20. The method as claimed in at least any one of claims 13 to 19, c h a r a c t e r i z e d in that a mode of the embedded system is provided in which only either the write access operations or the read access operations of the CPU are rerouted to the communication module, and the other access operations of the CPU to the memory are logged actively by the CPU into the external memory.

Abstract:

Device and Method for Analyzing Embedded Systems

~~The invention discloses~~ Disclosed is an analysis device for an embedded system (9) ~~comprising~~ including a CPU (1), a CPU bus (2) and a memory (3). The embedded system has at least one communication module (4) for the input or output of analysis data by way of a test interface (5). The communication module permits the internal memory and the input and output access operations of the embedded system to be monitored and/or logged without using the clock cycles of the CPU (1).

~~(Figure 1)~~